SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY

(AUTONOMOUS)
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QUESTION BANK (DESCRIPTIVE)

Subject with Code	**VLSI DESIGN (23EC0421)**	**Course & Branch**	**B.Tech – ECE**
Year & Sem	**III & II**	**Regulation**	**R23**

UNIT - I

INTRODUCTION

1	**a)**	Define MOS technology.	**[L1][CO1]**	**[2M]**
	b)	What are the basic steps involved in MOS/CMOS fabrication?	**[L1][CO1]**	**[2M]**
	c)	What is BiCMOS technology?	**[L1][CO1]**	**[2M]**
	d)	Define figure of merit (ω_0) in MOS devices.	**[L1][CO1]**	**[2M]**
	e)	Define transconductance (gm) in a MOSFET.	**[L1][CO1]**	**[2M]**
2	**a)**	Illustrate about basic MOS transistors.	**[L2][CO1]**	**[5M]**
	b)	Compare different modes in NMOS Transistor.	**[L4][CO1]**	**[5M]**
3	**a)**	Define Metal Oxide Semiconductor VLSI Technology.	**[L1][CO1]**	**[5M]**
	b)	List the advantages and disadvantages of IC.	**[L1[CO1]**	**[5M]**
4		Illustrate the steps involved in NMOS fabrication process with neat sketches.	**[L2][CO2]**	**[10M]**
5		Explain the steps involved in P-Well CMOS fabrication process with neat sketches.	**[L2][CO2]**	**[10M]**
6	**a)**	Compare CMOS with bipolar technology in different aspects.	**[L4][CO1]**	**[5M]**
	b)	State the different types of CMOS Process and illustrate the additional steps involved in Twin Tub Process.	**[L2][CO2]**	**[5M]**
7		Determine the relationship between I_{ds} & V_{ds} in non-saturated region.	**[L3][CO2]**	**[10M]**
8	**a)**	Derive the relationship between I_{ds} & V_{ds} in saturated region.	**[L1][CO2]**	**[5M]**
	b)	Define pass transistor with example.	**[L1][CO2]**	**[5M]**
9	**a)**	Define output conductance and figure of merit.	**[L1][CO2]**	**[5M]**
	b)	Show the circuit diagram of BiCMOS inverter and explain its operation.	**[L2][CO2]**	**[5M]**
10	**a)**	What are the different forms of Pull Up Loads? Which is the best choice for realization?	**[L2][CO2]**	**[5M]**
	b)	Derive the expression for threshold voltage for MOS transistors.	**[L2][CO2]**	**[5M]**
11	**a)**	Explain in detail about Transconductance.	**[L2][CO2]**	**[5M]**
	b)	Summarize the evolution of microelectronics.	**[L2][CO1]**	**[5M]**

UNIT - II

VLSI Circuit Design Processes

1	**a)**	What is meant by VLSI Design Flow?	**[L1][CO3]**	**[2M]**
	b)	What are MOS layers and why are they important?	**[L1][CO3]**	**[2M]**
	c)	What are design rules in VLSI layout?	**[L1][CO3]**	**[2M]**
	d)	Mention two advantages of scaling MOS circuits.	**[L1][CO3]**	**[2M]**
	e)	State two limitations of MOS scaling.	**[L1][CO3]**	**[2M]**
2	**a)**	Explain the steps involved in VLSI Design flow.	**[L2][CO3]**	**[5M]**
	b)	Construct the stick diagram of a 2-input CMOS NAND gate.	**[L3][CO3]**	**[5M]**
3	**a)**	What are lambda-based design rules? Explain.	**[L2][CO3]**	**[5M]**
	b)	Illustrate design rules for wires and MOS transistors.	**[L2][CO3]**	**[5M]**
4	**a)**	Explain the basic NMOS inverter circuit with neat diagram and its operation.	**[L2][CO3]**	**[5M]**
	b)	Draw the layout diagram of NMOS inverter circuit such that both input and output points are connected with Polysilicon layer.	**[L3][CO3]**	**[5M]**
5	**a)**	Explain about Stick diagram with one example.	**[L2][CO3]**	**[5M]**
	b)	Sketch the layout diagram for 2-input CMOS NAND gate.	**[L3][CO3]**	**[5M]**
6	**a)**	Explain the basic CMOS inverter circuit with neat diagram and its operation.	**[L2][CO3]**	**[5M]**
	b)	Sketch the layout diagram for CMOS inverter.	**[L3][CO3]**	**[5M]**
7	**a)**	Construct stick diagram for $\boldsymbol{Y} = (\boldsymbol{AB} + \boldsymbol{CD})$ in NMOS design style.	**[L3][CO3]**	**[5M]**
	b)	Construct the layout diagram for 2-input CMOS NOR gate.	**[L3][CO3]**	**[5M]**
8	**a)**	Construct layout diagram for the logic equations in CMOS logic. (i) $\boldsymbol{Y} = (\overline{\boldsymbol{A} + \boldsymbol{B}})\boldsymbol{C}$ (ii) Z= $(\overline{\boldsymbol{AB} + \boldsymbol{CD}})\boldsymbol{E}$	**[L3][CO3]**	**[5M]**
	b)	Illustrate λ-design rules for contact cuts.	**[L2][CO3]**	**[5M]**
9	**a)**	How a P-MOS transistor forms in lambda-based design rules? Explain.	**[L2][CO3]**	**[5M]**
	b)	Illustrate stick diagram of AND-OR-INVERTER in CMOS design Style.	**[L2][CO3]**	**[5M]**
10	**a)**	Explain about Implant and demarcation line in stick diagrams with neat sketches.	**[L2][CO3]**	**[5M]**
	b)	Construct the stick diagram for 2-input CMOS XOR gate.	**[L3][CO3]**	**[5M]**
11	**a)**	Explain Scaling of MOS Circuits.	**[L2][CO3]**	**[7M]**
	b)	Discuss its benefits.	**[L2][CO3]**	**[3M]**

UNIT - III

GATE LEVEL DESIGN & PHYSICAL DESIGN

1	**a)**	What is meant by Gate Level Design?	**[L1][CO4]**	**[2M]**
	b)	Define Switch Logic in VLSI design.	**[L1][CO4]**	**[2M]**
	c)	Define Sheet Resistance (R_s).	**[L1][CO5]**	**[2M]**
	d)	What is area capacitance in MOS circuits?	**[L1][CO5]**	**[2M]**
	e)	What does fan-in and fan-out mean in digital circuits?	**[L1][CO5]**	**[2M]**
2	**a)**	Explain Gate Level Design in VLSI.	**[L2][CO4]**	**[5M]**
	b)	Describe the CMOS implementation of basic logic gates.	**[L2][CO4]**	**[5M]**
3	**a)**	Explain the implementation of AOI and OAI using CMOS design style with neat sketches.	**[L1][CO4]**	**[6M]**
	b)	Sketch 2 x 1 mux using transmission gates.	**[L3][CO4]**	**[4M]**
4	**a)**	What is switch logic? Explain with an example.	**[L1][CO4]**	**[5M]**
	b)	Explain about pass transistors logic with an example.	**[L4][CO4]**	**[5M]**
5	**a)**	Explain dynamic CMOS logic circuit with an example.	**[L2][CO4]**	**[4M]**
	b)	Explain the following with an example i) Domino CMOS logic ii) NOR A logic.	**[L2][CO4]**	**[6M]**
6	**a)**	What is pseudo NMOS logic? Explain with an example	**[L1][CO4]**	**[5M]**
	b)	Construct 2-input NAND gate by using pseudo NMOS logic.	**[L3][CO4]**	**[5M]**
7	**a)**	Define Sheet Resistance (Rs).	**[L1][CO5]**	**[5M]**
	b)	Explain the importance of Sheet Resistance in MOS circuits.	**[L2][CO5]**	**[5M]**
8	**a)**	Define Inverter Delay in CMOS circuits.	**[L1][CO5]**	**[5M]**
	b)	Explain Area Capacitance in MOS technology.	**[L2][CO5]**	**[5M]**
9	**a)**	Explain the problem of driving large capacitive loads.	**[L2][CO5]**	**[5M]**
	b)	Describe techniques such as buffer insertion and tapered buffers.	**[L2][CO5]**	**[5M]**
10	**a)**	Explain Wiring Capacitances in VLSI circuits.	**[L2][CO5]**	**[5M]**
	b)	Discuss their effect on delay, noise, and signal integrity.	**[L2][CO5]**	**[5M]**
11	**a)**	Define Fan-in and Fan-out in digital circuits.	**[L1][CO5]**	**[5M]**
	b)	Analyze their impact on speed, power consumption, and reliability.	**[L4][CO5]**	**[5M]**

UNIT – IV

SUBSYSTEM DESIGN

1	**a)**	List any four functional blocks inside an ALU and briefly state their purpose.	[L2][CO4]	**[2M]**
	b)	What are the main parameters influencing low power design in VLSI?	[L2][CO4]	**[2M]**
	c)	Differentiate between FPGA and CPLD architectures based on logic structure and configuration.	[L4][CO5]	**[2M]**
	d)	What is standard cell design?	[L1][CO4]	**[2M]**
	e)	What is the function of a shifter in digital systems?	[L1][CO5]	**[2M]**
2	**a)**	Design a Carry Look-Ahead Adder.	[L4][CO5]	**[6M]**
	b)	Compare Carry Look-Ahead Adder with Ripple Carry Adder.	[L4][CO5]	**[4M]**
3	**a)**	Explain in detail about parity generator.	[L2][CO2]	**[5M]**
	b)	Explain the design of a 4-bit Shifter.	[L3][CO5]	**[5M]**
4		Explain the architecture of an Arithmetic Logic Unit (ALU).	[L2][CO4]	**[10M]**
5		Discuss Array multiplier in detail. And design 4*4 multiplier.	[L4][CO5]	**[10M]**
6	**a)**	Design a 4-bit Magnitude Comparator.	[L1][CO4]	**[5M]**
	b)	Design a Comparator using a tree-based logic structure.	[L3][CO5]	**[5M]**
7	**a)**	Explain about the principle and functions of FPGA.	[L3][CO5]	**[5M]**
	b)	Explain the Semi-Custom and Full-Custom methodologies.	[L4][CO5]	**[5M]**
8	**a)**	Explain CPLD architecture.	[L3][CO5]	**[5M]**
	b)	Design the flow in Semi-Custom approach.	[L3][CO5]	**[5M]**
9	**a)**	Derive dynamic & static power equations.	[L5][CO4]	**[5M]**
	b)	Discuss the low-power techniques in power equations.	[L4][CO5]	**[5M]**
10	**a)**	Discuss the advantages and limitations of Full-Custom design methodology.	[L4][CO5]	**[5M]**
	b)	Derive the dynamic power consumption equation in CMOS circuits.	[L3][CO4]	**[5M]**
11		Design a 4-bit Counter sub circuit design.	[L5][CO4]	**[10M]**

UNIT –V
CMOS TESTING

1	**a)**	What is the difference between testing combinational and sequential circuits?	**[L2][CO6]**	**[2M]**
	b)	Define scan chain in scan design technique.	**[L1][CO6]**	**[2M]**
	c)	State any four practical design-for-test (DFT) guidelines used in VLSI design.	**[L4][CO6]**	**[2M]**
	d)	Why is testing necessary in CMOS VLSI circuits?	**[L1][CO6]**	**[2M]**
	e)	What is Built-In Self-Test (BIST)?	**[L2][CO6]**	**[2M]**
2	**a)**	Discuss various fault models used in testing combinational logic circuits.	**[L4][CO6]**	**[5M]**
	b)	Explain testing of combinational logic circuits.	**[L3][CO6]**	**[5M]**
3	**a)**	What is the need for testing CMOS.	**[L2][CO6]**	**[5M]**
	b)	Explain the concept of Design for Testability (DFT).	**[L3][CO5]**	**[5M]**
4	**a)**	Discuss Logic BIST (LBIST).	**[L4][CO6]**	**[5M]**
	b)	Explain Memory BIST (MBIST).	**[L3][CO6]**	**[5M]**
5	**a)**	Explain the procedure to do manufacturing test in detail.	**[L3][CO6]**	**[5M]**
	b)	Describe the testing methodology for sequential circuits using scan insertion.	**[L2][CO4]**	**[5M]**
6	**a)**	Explain the trade-offs between area overhead, performance degradation, and fault coverage in DFT techniques.	**[L5][CO6]**	**[8M]**
	b)	Define ATPG.	**[L1][CO5]**	**[2M]**
7	**a)**	Describe Built-In Self-Repair (BISR) in memory testing.	**[L3][CO6]**	**[8M]**
	b)	What is Ad Hoc testing?	**[L2][CO6]**	**[2M]**
8	**a)**	Explain signature analysis in BIST.	**[L3][CO6]**	**[5M]**
	b)	Explain the difference between functional testing and structural testing.	**[L4][CO6]**	**[5M]**
9	**a)**	Discuss various types of delay faults in CMOS circuits.	**[L4][CO6]**	**[5M]**
	b)	Illustrate the scan-based technique.	**[L2][CO3]**	**[5M]**
10	**a)**	What is LFSR?	**[L3][CO6]**	**[2M]**
	b)	Describe the architecture and working of a Linear Feedback Shift Register (LFSR).	**[L3][CO6]**	**[8M]**
11	**a)**	What are the types of self-test approaches?	**[L2][CO6]**	**[5M]**
	b)	Explain the role of controllability and observability in VLSI testing.	**[L4][CO6]**	**[5M]**